Transmission electron microscopy studies of the bonded SiC-SiC interface

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SiC is a promising material for high-power and high-temperature electronics due to its chemical inertness, high thermal conductivity (~5 W cm^{-1} K^{-1}), and wide band gap (2.4–3.3 eV, depending on the polytype). SiC diodes, field effect transistors, as well as bipolar homojunction transistors fabricated to date, showed that their performance exceeds even theoretical limits of Si and GaAs counterparts [1, 2]. Heterojunction devices can offer improved efficiency compared to the homojunction devices [3]. Koitzsch *et al.* suggested a wafer-bonding technique [4] to fabricate higher efficiency heterojunction devices using different SiC polytypes [5]. The interface obtained during bonding will determine the device operation. This work focuses on transmission electron microscopy (TEM) studies of the bonded SiC/SiC interfaces.

In all bonding experiments, on-axis Si-face (0001) SiC wafers (either 6H or 4H) obtained from Cree, Inc., were used. The root-mean-square (RMS) surface roughness of as-received SiC wafers was measured by atomic force microscopy (AFM) using a Digital Instruments D3000 microscope. These measurements revealed an RMS surface roughness of ~2 nm, which is higher than the 0.5 nm limit required for room temperature bonding [4]. Fig. 1 shows an AFM image of a typical SiC surface. Dark lines in the image correspond to the polishing scratches.

The macroscopic surface roughness (waviness) of SiC wafers was studied on a Zygo GPI XP Laser Interferometer. Although the observed surface profile (Fig. 2) varied from wafer-to-wafer, the value for the peak-to-valley waviness was consistently 5–7 μm for our 12 × 22 mm^2 samples. This is similar to the waviness of similarly sized Si samples, which was measured to be 3–6 μm. This level of macroscopic flatness was found suitable for the well-established Si/Si (or Si/SiO_2) wafer bonding and thus was not expected to create any major obstacles in bonding of SiC wafers.

To prepare particle-free samples for our bonding experiments, all wet cleaning procedures were performed in a class 100 clean-room environment. SiC samples were ultrasonically cleaned in BakerClean® solution for 10 min, in 10% hydrofluoric acid for 10 min, in BakerClean® solution for another 10 min, in deionized water for 1–3 min, and finally blow-dried with nitrogen. The final cleaning procedure was performed in a UHV chamber with a base pressure of ~10^{-9} Torr. Inside this chamber, SiC samples were desorbed for several hours at 300–500 °C and for ~1 hr at 1100 °C. The chemical analysis of the sample surface using *in-situ* X-Ray Photoelectron Spectroscopy confirmed the effectiveness of the employed cleaning procedure in removing native oxide. Results of the analysis are reported separately [6]. Minimization of the time between the wet and dry cleaning procedures was found to be favorable for effective removal of surface contaminants. Forbeaux *et al.* [7] observed graphitization of Si-terminated SiC under annealing in vacuum at temperatures above 1100 °C. Although we used similar procedure we did not observe any surface graphitization as confirmed by XPS [6]. All XPS experiments were conducted in an ultra high vacuum chamber (base pressure $<3 \times 10^{-10}$ Torr), equipped with a Clam II hemispherical electron analyzer. The AFM studies performed on the cleaned SiC samples did not reveal any changes in the surface topography.

UHV wafer bonding was performed in a custom-built, UHV bonding chamber, under a uniaxial stress of 20 MPa for a period of 15 hr in a temperature range of 800–1100 °C. Samples bonded at 1100 °C were analyzed using TEM. Standard preparation techniques were used for the preparation of XTEM samples: mechanical polishing to a thickness of 40 μm, dimpling, and ion milling. A 200 kV field-emission TEM (JEOL 2010F) with an imaging filter (Gatan GIF) was used in these studies.

TEM images revealed the presence of an atomically abrupt interface between the bonded wafers without any visible intermediate layer between them. This indicated that the removal of SiO_2 was sufficient and suggested that the employed wafer cleaning procedure preserved the crystalline structure of the SiC surface. Figs 3–5 show high-resolution TEM images of SiC wafers bonded at 1100 °C. Occasionally, the interface contained thin (up to 2 nm in thickness) amorphous regions of less than 200 nm in length. These regions occupied less than 5% of the observed area and were not expected to significantly influence the macroscopic characteristics of the junction [6].

The bonded couples possessed various degrees of twist relative to each other about the z-axis (in other words, they were azimuthally misaligned). This

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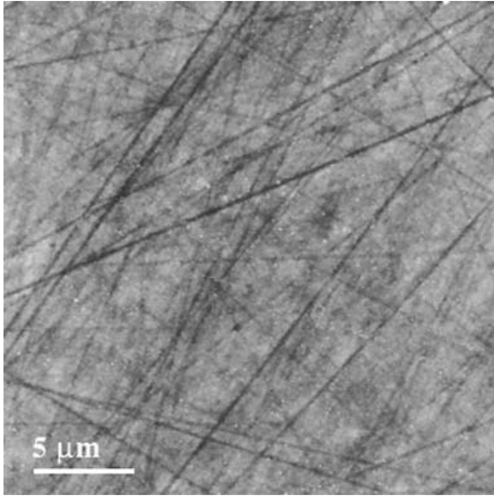


Figure 1 AFM surface analysis of a SiC wafer shows polishing scratches. Estimated RMS surface roughness is ∼2 nm.

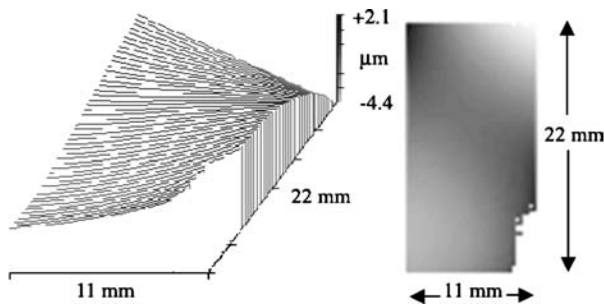
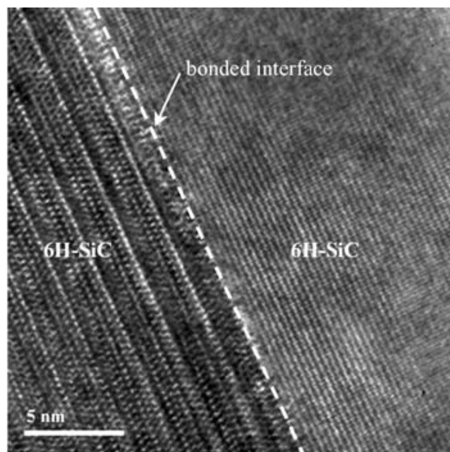
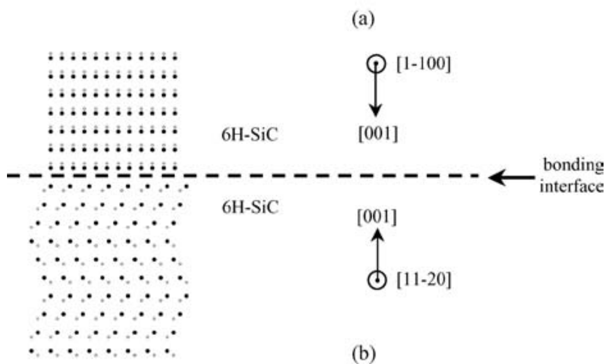


Figure 2 SiC surface analysis by Interferometry. Estimated long range waviness is 5–7 μm.

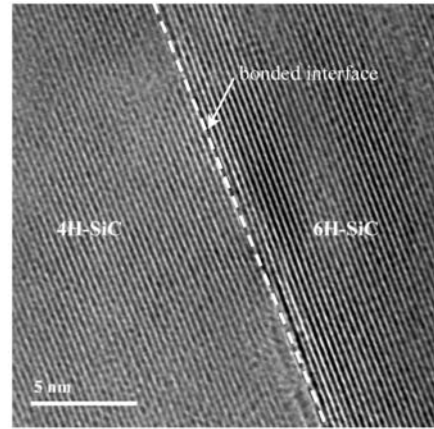


(a)

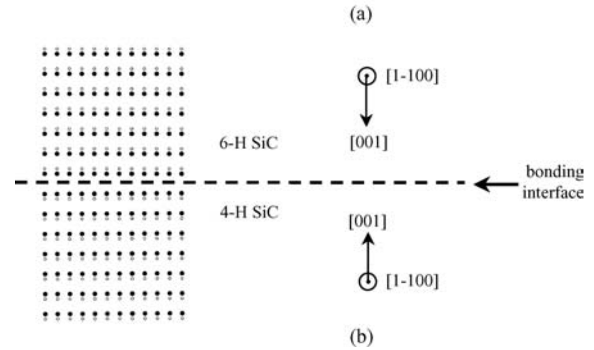


(b)

Figure 3 HRTEM image of 6H–SiC bonded to 6H–SiC at 1100 °C (a). Relation of crystal axes between the SiC wafers with a schematic of the lattice structure (b).

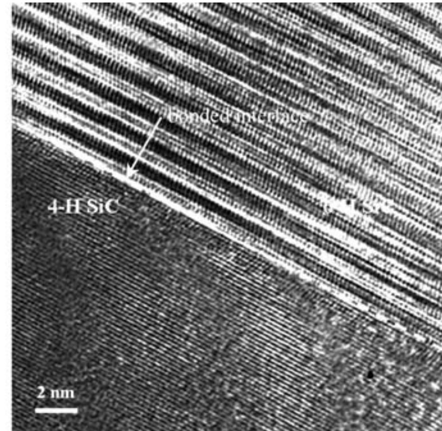


(a)

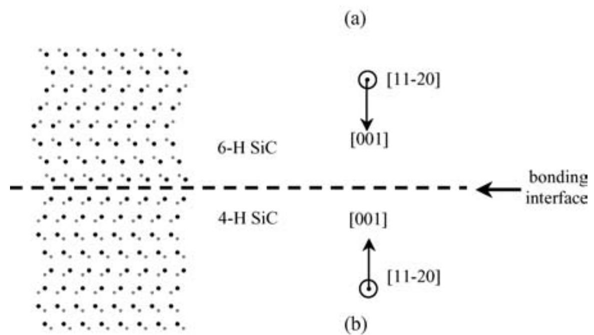


(b)

Figure 4 HRTEM image of 6H–SiC bonded to 4H–SiC at 1100 °C (a). Relation of crystal axes between these SiC wafers with a schematic of the lattice structure (b).



(a)



(b)

Figure 5 HRTEM image of 6H–SiC bonded to 4H–SiC at 1100 °C; 4H–SiC is ∼2 ° off the Zone Axis (a). Relation of crystal axes between the SiC wafers with a schematic of the lattice structure (b).

misalignment represents a twist boundary, which can be envisioned as a regular array of screw dislocations with Burger's vectors parallel to the plane of the boundary (see the book by W.T. Read [8]). The lattice parameters

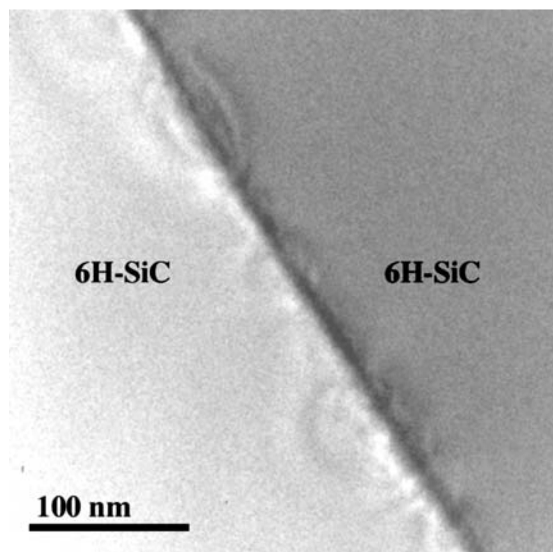


Figure 6 TEM image of the strain field created at the bonded interface of a 6H–SiC/6H–SiC sample due to the azimuthal twist of ∼0.3 ° between the wafers.

of the wafers in the x–y plane and the angle of the twist determine the spacing between the dislocations. The distance between dislocations was found to be in a reasonable (for a hexagonal system) agreement with the calculated values. For example, in case of 6H–SiC/6H–SiC wafers bonded with an azimuthal twist of ∼0.3 °, the spacing between the most strained areas (presumably projections of screw dislocations) was found to be 20–60 nm (see Fig. 6) when observed in TEM along the ⟨11–20⟩ direction; this is in a relatively good agreement with the estimated spacing of ∼30 nm.

The two-beam images of the fused specimens clearly indicated an absence of threading dislocations. These dislocations would create a strain field that would appear as contrast fringes away from the interface. The absence of dislocations and planar defects emanating from the interface was a bit surprising for the described high temperature bonding process. Several factors might have helped to preserve the SiC crystalline quality: (1) due to the similarity of the coefficients of thermal expansion in 6H–SiC and 4H–SiC, thermal stress was minimized, (2) the applied mechanical stress was normal to the slip plane of SiC (basal plane), and (3) SiC has a high melting point (more than two times the processing temperature) and mechanical properties superior to those of Si and most other semiconductor materials.

In summary, commercially available SiC wafers with an RMS roughness of 2 nm were cleaned on the atomic level and successfully bonded in ultra high vacuum at 20 MPa of applied uniaxial pressure at temperatures as low as 800 °C. TEM studies revealed that wafer fusion enables fabrication of abrupt, atomically clean heterointerfaces using commercially available SiC wafers.

Acknowledgments

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